SILICON CONTROLLED RECTIFIER ELECTROSTATIC DISCHARGE PROTECTION DEVICE WITH EXTERNAL ON-CHIP TRIGGERING AND COMPACT INTERNAL DIMENSIONS FOR FAST TRIGGERING

CROSS REFERENCES:

[0001] This patent application claims the benefit of US. Provisional Applications, serial number 60/280,345, filed March 30, 2001; serial number 60/246,123, filed November 6, 2000; and serial number 60/266,171, filed February 2, 2001, the contents of which are incorporated by reference herein.

FIELD OF THE INVENTION:

[0002] This invention generally relates to the field of electrostatic discharge (ESD) protection circuitry, and more specifically, improvements for silicon controlled rectifier (SCR) structures in the protection circuitry of an integrated circuit (IC).

BACKGROUND OF THE INVENTION

[0003] Integrated circuits (IC's) and other semiconductor devices are extremely sensitive to the high voltages that may be generated by contact with an ESD event. As such, electrostatic discharge (ESD) protection circuitry is essential for integrated circuits. An ESD event commonly results from the discharge of a high voltage potential (typically, several kilovolts) and leads to pulses of high current (several amperes) of a short duration (typically, 100 nanoseconds). An ESD event is generated within an IC, illustratively, by human contact with the leads of the IC or by electrically charged machinery being discharged in other leads of an IC. During installation of integrated circuits into products, these electrostatic discharges may destroy the IC's and thus require expensive repairs on the products, which could have been avoided by providing a mechanism for dissipation of the electrostatic discharge to which the IC may have been subjected.

[0004] The ESD problem has been especially pronounced in complementary metal oxide semiconductor (CMOS) field effect transistors. To protect against

these over-voltage conditions, silicon controlled rectifiers (SCR) and other protection devices such as the grounded-gate NMOS have been incorporated within the circuitry of the CMOS IC to provide a discharge path for the high current produced by the discharge of the high electrostatic potential. Prior to an ESD event, the SCR is in a nonconductive state. Once the high voltage of an ESD event is encountered, the SCR then changes to a conductive state to shunt the current to ground. The SCR maintains this conductive state until the voltage is discharged to a safe level.

[0005] FIG. 1A depicts a schematic diagram of a prior art SCR included within an integrated circuit to provide ESD protection as illustratively provided in US Patents 5,465,189 and US Patent 5,502,317. In particular, an illustrative prior art integrated circuit 100 has an SCR protection circuit 101 connected from a pad 148 to ground. The pad 148 is also connected to the protected circuitry of the IC, optionally through a current limiting resistor R_L. The SCR protection circuit 101 comprises a trigger device 105 and an SCR 102. The SCR 102 further comprises a NPN transistor T1 131 and a PNP transistor T2 132. In particular, the SCR protection device 101 includes an anode122, which is connected to the pad 148, and to one side of a resistor R_{B2} 142. The resistor R_{B2} 142 represents the resistance of the N-well, which is seen at the base of a PNP transistor of the SCR 102, as is discussed in further detail below. Additionally, the anode 122 is coupled to an emitter 108 of a PNP transistor T2 132, which is parallel to the N-well resistance R_{B2} 142. A first node 134 includes the base of the PNP transistor T2 132, the other side of the resistor R_{B2} 142, and the collector of the NPN transistor T1 131. Additionally, the collector 106 of the PNP transistor T2 132 is connected to a second node 136, which is also connected to the base 106 of the NPN transistor T1 131, and to one side of a resistor R_{B1} 141. The other side of resistor R_{B1} 141 is connected to a third node 124 that is grounded, and which serves as the cathode. Furthermore, the emitter 112 of the NPN transistor T1 131 is also connected to the grounded third node 124.

[0006] The triggering device 105 is illustratively a grounded gate NMOS (GGNMOS) transistor, which has its source 127 and gate 126 coupled to ground.

Additionally, the drain 125 and source 127 of the GGNMOS transistor 105 are respectively coupled to the collector 110 and the emitter 112 of the NPN transistor T1 131. Furthermore, the gate 126 and source 127 of the GGNMOS transistor are also connected to the grounded third node 124 (i.e., cathode of the SCR).

[0007] FIG. 1B depicts a cross-sectional view of a prior art low voltage triggering SCR (LVTSCR) device as depicted in FIG. 1A. Furthermore, FIG. 1B illustratively includes the schematic diagram of the SCR circuit as related to the P and N doped regions of the IC 100. Specifically, the integrated circuit 100 includes a P-type substrate 103 into which an N-well 104 and P-well 106 are formed adjacent to each other. A junction 107 is formed at the adjoining boundary of the N-well 104 and the P-well 106.

[0008] Within the N-well 104, a first P+ region 108 is formed. Furthermore, within the P-well 106, a first N+ region 112 and a second P+ region 114 are formed thereupon. In addition, a second N+ region 110 is formed over both the P-well 106 and N-well 104 regions such that the second N+ region 110 overlaps the junction 107 of the P-well and N-well regions 106 and 104. The regions denoted P+ an N+ are regions having higher doping levels than the N-well and P-well regions 104 and 106.

[0009] Shallow trench isolation (STI) is used in most state-of-the-art CMOS processing technologies to laterally separate the high-doped regions. Shallow trench isolation is performed prior to forming the high P+ and N+ doped regions. In particular, trenches are etched in specific areas from the silicon surface, and an insulator material (e.g., silicon dioxide (SiO_2)) is deposited to fill the trenches. A gate dielectric layer such as silicon dioxide (SiO_2) 130 is grown over the parts of the surface exposing bare silicon. A gate electrode material (e.g. poly silicon) is deposited over the entire surface. The gate electrode material and the gate dielectric are structured by a photo-lithographical masking followed by an etching step. After the masking and etching steps, only the photo patterned area of the gate dielectric 130 and the gate electrode 128 remain, as illustrated. Then, the

silicon between the STI receives ion implants to form the high-doped P and N regions as discussed above.

[0010] Specifically, after performing the STI and creating the high-doped regions, a first STI region 116_1 is positioned illustratively to the left of the first P+ doped region 108. Additionally, a second STI region 116_2 is positioned between the first P+ region 108 and the second N+ region 110. Furthermore, a third STI region 116_3 is positioned between the first N+ region 112 and the second P+ region 114, and a fourth STI region 116_4 is positioned to the left of the second P+ region 114.

[0011] The gate 126 of the GGNMOS transistor 105 separates the first and second N+ regions 112 and 110. Furthermore, the GGNMOS transistor 105 is used to "trigger", i.e., turn on the SCR. In particular, the GGNMOS transistor 105 is an N-channel MOS transistor, which includes a drain and source, which are respectively formed by the second N+ region 110 and the first N+ region 112. The NMOS-channel is formed at the surface of the P-well region 120 between the first and second N+ regions 112 and 110. Additionally, since the gate 126 is grounded, the P-well region 120 is prevented from forming the NMOS-channel between the first and second N+ regions 112 and 110, thereby preserving the functionality of the SCR's bipolar transistor T1 131.

[0012] The NPN transistor T1 131 has its emitter formed by the first N+ region 112, the base formed by the P-well 106, and the collector formed by the N-well 104, which is electrically in parallel with the second N+ region 110 (NMOS drain). The PNP transistor T2 132 has its emitter formed by the first P+ region 108, the base formed by the N-well 104 and the second N+ region 110, and the collector formed by the P-well 106. It should be noted that the N-well 104 and the drain region 110 define both the collector of the NPN transistor T1 131 and the base of the PNP transistor T2 132.

[0013] The first P+ region 108 is spaced apart from the second N+ region 110. If the N-well 104 is optionally connected by an additional N+ region (not shown) to the anode 122, then the N-well resistance R_{B2} 142 is defined therebetween (For example, an additional N+ region in the N-well 104).

Otherwise, if the N-well is floating the resistor R_{B2} 142 is not defined (as drawn in phantom in FIG. 1B). As such, the well resistance R_{B2} 142 is the base resistance of the PNP transistor T2 132, and has a resistance value that depends on the N-type material resistivity value. The N-type material includes the level of doping, as well as the length and cross-sectional area of the N-well 104 (i.e., base). Typically, the resistance R_{B2} 142 is in the range of 500 Ohm to 5000 Ohms, or it is an open if the N-well is floating (as shown in FIG. 1B). Furthermore, since the second N+ region 110 is coupled to the N-well 104, the N+ region 110 also functions as part of the base of the PNP transistor T2 132. Likewise, the P-well region 106 forms the base of the NPN transistor T1 131 and also has a substrate resistance R_{B1} 141. Typically, the resistance R_{B1} 141 is in the range of 500 to 5000 Ohms.

[0014] The anode 122, cathode 124, and a substrate-tie 125 are respectively coupled to the first P+ region 108, the first N+ region 112, and the second P+ region 114 through silicide layers 118_A, 118_C, and 118_S (collectively silicide layers 118). Furthermore, one skilled in the art will recognize that there are older process technologies that do not have the silicide layer. As such, the anode 122, cathode 124, and substrate-tie 125 are directly connected to the N+ and P+ regions. The silicide layers 118 are formed such that a conductive metal (typically, tungsten or cobalt) is deposited as a very shallow film over the entire IC wafer. A heating step follows and the metal reacts only with the silicon surface to form an alloy of silicon and metal ("silicide"). The other surfaces such as oxides or nitrides do not react with the metal. The non-reacted metal is selectively etched away so that only the silicide layers remain on the silicon. The silicide layers 118 serve as a conductive bonding material respectively between each metal contact 121_A, 121_C, and 121_S (collectively metal contacts 121) of the anode 122, cathode 124, and substrate-tie 125. FIG. 1B depicts a typical implementation where silicide formation is blocked in part of the NMOS 105.

[0015] In operation, the protective SCR circuit 102, which comprises the NPN and PNP transistors T1 131 and T2 132, will not conduct current between the anode 122 and the grounded cathode 124. That is, the SCR 102 is turned off,

since there is no high voltage (e.g., ESD voltage) applied to the SCR 102, but only the regular signal voltage of the IC. Once an ESD event occurs at the pad 148, a voltage potential appears on the anode 122. Furthermore, the voltage potential created by the ESD event is transferred in part to the N+ region 110 via the N-well 104. That is, the anode 122, P+ region 108, N-well region 104, and N+ region 110 are connected in series such that a voltage will form at the N+ region 110.

[0016] The N+ region 110 and the P-well 106 form a diode that functions as a triggering mechanism for the SCR 102. In particular, the N+ region 110 and the P-well region 120 act as a diode D_R. The diode D_R (drawn in phantom) will conduct when the voltage across the diode exceeds the diode reverse breakdown voltage, typically 6-10 volts. That is, once the voltage transferred in part from the ESD event on the N+ region 110 exceeds the diode D_R reverse breakdown voltage, an avalanche effect occurs such that holes and electrons are generated in the PN-junction of the diode D_R. The holes flow into the P-well regions 120 and 119 of the P-well 106 and to the grounded P+ region 114. The potential in the P-well regions 120 and 119 increases and electrons flow from the N+ region 112 (emitter) mainly into the P-well region 120 and also into the part of the P-well region denoted 119. The flow of minority carriers (electrons) into the P-well region 120 causes the SCR 102 to trigger. Likewise, the electrons generated in the PN-junction of the diode D_R will flow into the N-well 104 and cause the P+ emitter 108 to inject minority carriers (holes) into the N-well 104.

[0017] Specifically, the majority carriers (i.e., holes) generated at the PN-junction of the N+ region 110 and the P-well region 120 recombine in the P-well regions 120 and 119 with the minority carriers (electrons) injected from the N+ region 112 (emitter). As such, the base of the NPN transistor T1 131 draws current, illustratively at the gate G1 in the P-well region 120, which subsequently turns on the NPN transistor T1 131. Furthermore, the collector of the NPN transistor T1 131 is coupled to the base of the PNP transistor T2 132, which turns on the PNP transistor T2 132. The collector current of the NPN transistor T1 131 equals the current gain of T1 131 (β_1) times the base current of the

transistor T1 131. The current gain β_1 is dependent on the geometrical dimensions and the doping levels in the base and emitter of the NPN transistor T1 131. Likewise, a current gain β_2 is dependent on the geometrical dimensions and the doping level of the PNP transistor T2 132.

[0018] As such, once the NPN transistor T1 131 is turned on, the T1 131 collector provides the base current to the PNP transistor T2 132. Therefore, the base current of the PNP transistor T2 132 is greater than the base current of the NPN transistor T1 131. Moreover, the current gain β_2 of the PNP transistor T2 132 is realized as the T2 132 collector current, which is then fed back to the base of the NPN transistor T1 131, thereby amplifying the base current of the NPN transistor T1 131. This amplification of the base currents in the SCR 102 progressively continues to increase in a loop between both transistors T1 131 and T2 132. Therefore, the conduction in a turned on SCR is also called a "regenerative process".

[0019] The SCR 102 becomes highly conductive and sustains the current flow with a very small voltage drop between the anode and cathode (typically, 1-2V). Accordingly, once the SCR 102 is turned on, the current from the ESD event passes from anode 122 to the grounded cathode 124. As such, the SCR 102 protects the remaining portion of the IC circuitry 100. Once the ESD event has been discharged from the anode 122 to the cathode 124, the SCR 102 turns off because it cannot sustain its regenerative conduction mode.

[0020] It is critical to discharge the ESD event as quickly as possible to prevent damage to the circuitry of the IC, as well as to the protective SCR itself. In the above prior art LVTSCR, the NMOS transistor 105 is integrated within the SCR 102. The N+ region diffusion 110 inserted as an integrated trigger means is disadvantageous due to the excessive base widths of the NPN transistor T1 131 and the PNP transistor T2 132. Therefore, the large lateral T1 and T2 transistor dimensions, due to the insertion of the N+ diffusion and the high recombination of charge carriers, results in slow SCR triggering. In particular, the N+ region 110 ("trigger diffusion region"), which is also part of the base of the PNP transistor T2 132, deteriorates the current gain of this part of T2 132. That is, since the N-well

region 104 has the higher doped N+ region 110 disposed therein, the overall current gain β_2 of the transistor T2 132 is reduced, which may impede (e.g., delay or prevent) the SCR 102 from triggering during an ESD event. Therefore, there is a need in the art for a fast triggering SCR protection device having a reliable and controllable triggering mechanism.

SUMMARY OF INVENTION

[0021] The disadvantages heretofore associated with the prior art are overcome by the present invention of a silicon controlled rectifier electrostatic discharge protection circuit with external on-chip triggering and compact internal dimensions for fast triggering. The ESD protection circuit includes a silicon controlled rectifier (SCR) having an anode coupled to the protected circuitry and a cathode coupled to ground, where the cathode has at least one high-doped region. At least one trigger-tap is disposed proximate to the at least one high-doped region and an external on-chip triggering device is coupled to the trigger-tap and the protected circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] FIG. 1A depicts a schematic diagram of a prior art SCR included within an integrated circuit to provide ESD protection;

[0023] FIG. 1B depicts a cross-sectional view of a prior art low voltage triggering SCR (LVTSCR) device of FIG. 1A;

[0024] FIG. 2A depicts four illustrative schematic diagram embodiments of a NMOS triggered SCR ESD protection device of the present invention;

[0025] FIG. 2B depicts an illustrative schematic diagram of a PMOS triggered SCR ESD protection device of the present invention;

[0026] FIG. 3 depicts a cross-sectional view of a first embodiment of a SCR of the NMOS or PMOS-triggered SCR ESD protection device of FIGS. 2A and 2B;

[0027] FIG. 4 depicts a top view of the first embodiment of the NMOS-triggered SCR ESD protection device of FIG. 2A;

[0028] FIG. 5 depicts a top view of a second embodiment of the PMOS-triggered SCR ESD protection device of FIG. 2B;

[0029] FIG. 6 depicts a cross-sectional view of a second embodiment of a SCR of the NMOS or PMOS-triggered SCR ESD protection device of FIGS. 2A and 2B;

[0030] FIG. 7 depicts a cross-sectional view of a back-end ballasted, NMOS-trigger device; and

[0031] FIG. 8 depicts a top view of a SCR ESD protection device having a back-end ballasted, NMOS-trigger device.

[0032] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION OF THE INVENTION

[0033] The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits (ICs). The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections and layouts of portions of an IC during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention. Furthermore, where possible, the figures illustratively include a schematic diagram of the circuitry (e.g., an SCR circuit) as related to the P and N-type doped regions of the integrated circuit.

[0034] The present invention is described with reference to CMOS devices. However, those of ordinary skill in the art will appreciate that selecting different dopant types and adjusting concentrations allows the invention to be applied to NMOS, PMOS, and other processes that are susceptible to damage caused by ESD.

[0035] FIG. 2A depicts four illustrative schematic diagram embodiments (A-D) of a NMOS triggered SCR ESD protection device 201 of the present invention.

Each of the embodiments in schematic diagrams A-D illustratively depicts an IC pad 148 coupled to a trigger device 205 and an SCR 202. An optional current limiting resistor R_L may be positioned between the circuitry to be protected and the SCR ESD protection device 201. The triggering device 205 and SCR 202 together serve as a protection device for the circuitry on an integrated circuit (IC) 200. In particular, the triggering device 205 and SCR 202 protect the IC circuitry from electrostatic discharges (ESD) that may occur at the pad 148, which is coupled to the IC circuitry. When turned on, the SCR 202 functions as a shunt to redirect any ESD currents from the pad 148 to ground. The trigger device 205 turns on, that is "triggers" the SCR 202 to quickly dissipate such over-voltage ESD condition.

[0036] Referring to the schematic diagram A of FIG. 2A, the SCR protection device 201 includes an anode 122, which is connected to the pad 148 and optionally to one side of a resistor R_{B2} 242. The resistor R_{B2} 242 represents a N-well resistance in a base of a transistor T2 232 of the SCR 202, which is discussed in further detail below. Additionally, the anode 122 is coupled to an emitter 108 of a PNP transistor T2 232, which is parallel to the N-well resistance R_{B2} 242. Optionally, a number of diodes D_S (drawn in phantom) may be coupled between the anode 122 and the emitter 108 of the PNP transistor T2 232. The serially connected diodes D_S (typically 1-4 diodes) are optionally provided to increase the holding voltage of the SCR as may be required to fulfill latch-up specifications.

[0037] A first node 134 includes the base of the PNP transistor T2 232, the other side of the resistor R_{B2} 242, and the collector of a NPN transistor T1 231. Additionally, the collector of the PNP transistor T2 232 is connected to a second node 136, which is also connected to the base of the NPN transistor T1 231, as well as to one side of a resistor R_{B1} 241, and into the trigger 205 (discussed below). The other side of resistor R_{B1} 241 is connected to a third node 124, which is grounded and serves as the cathode. The resistor R_{B1} 241 represents a substrate resistance in a base of a transistor T1 231 of the SCR 202, which is discussed in further detail below. Furthermore, the emitter of the PNP transistor

T1 231 is also connected to the grounded third node 124, which functions as a cathode.

[0038] The triggering device 205 in the schematic diagram A includes a NMOS transistor 206, where the gate is connected to the source and an external resistor 210. Specifically, the drain of the NMOS transistor 206 is coupled to the pad 148, the gate connected to the source to turn off any MOS current, and the source and the gate of the NMOS transistor 206 are coupled to the second node 136 in the SCR 202. Furthermore, the resistor 210 is coupled to the second node 136 on one end, and to the third node 124 on the other end. That is, the resistor 210 is external to the SCR transistors T1 231 and T2 232, and is provided in parallel to the intrinsic resistance R_{B1} 241 of the P-substrate 103 when no P-well is present, or the P-well 104. The resistor 210 is selected with a resistance value that is lower than the inherent base resistance R_{B1} 241, and serves as a shunt resistor for directing small amounts of current to ground. Therefore, resistor 210 provides a path for undesirable leakage currents between the source of the trigger device 205 and ground, which otherwise might unintentionally trigger the SCR 202. Furthermore, as recognized by those skilled in the art, the resistor 210 will control the so-called holding current of the SCR.

[0039] The remaining three schematics depicted in diagrams B-D of FIG. 2A are the same, except that the trigger device 205 is shown in various embodiments. For example, in schematic B, a NMOS transistor is provided with drain-bulk-gate coupling, i.e. the local bulk (p-well) and gate are connected and drain to bulk coupling is achieved by the drain to bulk capacitance (not shown in the figure). In schematic C, the NMOS is in an isolated P-well, and in schematic D, two cascoded NMOS transistors 206_1 and 206_2 are used as part of the triggering device 205. Furthermore, one skilled in the art will recognize that other triggering devices and configurations may be implemented, which are external to the SCR 202.

[0040] The coupled trigger NMOS transistor 206 (as shown in the schematics of FIG. 2A) allows the SCR 202 to turn on faster than the prior art LVTSCR device (see FIG 1A). Specifically, the drain of the NMOS transistor 206 is no

longer coupled to the collector of the NPN transistor T1 231 (also, base of the PNP transistor T2 232), which was used to provide a reverse biased breakdown voltage between the N^{+} region 110 (base) of the PNP transistor T2 232 and the P-well region 120 (base) of the NPN transistor T1 231. Rather, the source and the gate of the NMOS transistor 206 are coupled directly to the base of the NPN transistor T1 231, which is discussed below in detail with regard to FIGS. 3 and 4.

[0041] Furthermore, a person skilled in the art for which this invention pertains will understand that a PMOS triggered SCR ESD protection device may also be utilized. For example, FIG. 2B depicts an illustrative schematic diagram E representing a PMOS triggered SCR ESD protection device 201 of the present invention. Furthermore, a person skilled in the art will recognize that a PMOS transistor with drain-bulk-gate coupling, or two cascoded PMOS transistors, or other external triggering devices 205 may used as part of ESD protection device 201, as discussed above.

[0042] For purposes of clarity, the invention will be discussed as a NMOS triggered SCR as illustratively depicted in the schematic diagram A of FIG. 2A. FIG. 3 depicts a cross-sectional view of a SCR 202 of the NMOS-triggered SCR ESD protection device 201 of FIGS. 2A and 2B.

[0043] Specifically, the protection device 201 includes in part, a P-type substrate 303, into which an N-well 304 and P-well 306 is formed. The N-well 304 and P-well 306 are adjacent to each other and form a junction 307 at the adjoining boundary. Within the N-well 304, a first P+ region 308 is formed. Furthermore, within the P-well 306, a single N+ region 312 and a second P+ region 314 are formed thereupon. The regions denoted P+ and N+ are regions having higher doping levels than the N-well and P-well regions 304 and 306. Furthermore, it should be noted that there is no "second N+ region 110" formed over and overlapping the junction 307 between both the P-well 304 and N-well 306 regions, as shown in the prior art of FIG. 1B.

[0044] The illustrative schematic diagram in FIG. 3 represents the components of the SCR 202, which correspond to the schematic diagrams in

FIG. 2A. That is, FIG. 3 is illustrated and discussed as an SCR for an NMOS triggering device with the source and gate connected together. However, a person skilled in the art will understand that where a PMOS triggering device is used, the N- and P-type regions illustratively shown in FIG. 3 as well as the potentials and terminals are reversed. Referring to FIG. 3, the NPN transistor T1 231 is formed by the N+ region 312 (emitter), the P-well 306 (base) and the N-well 304 (collector). The PNP transistor T2 232 is formed by the P+ region 308 (emitter), the N-well region 304 (base), and the P-well region 306 (collector). It should be noted that the N-well 304 serves dual functions as the collector of the NPN transistor T1 231, as well as the base of the PNP transistor T2 232. Likewise, the P-well 306 serves dual functions as the collector of the PNP transistor T2 232, as well as the base for the NPN transistor T1 231. The second P+ region 314 forms the substrate-tie 125, which is usually connected to the cathode 124 and grounded.

[0045] The P-well 306 has an intrinsic resistance, which is observed as the well/substrate or as the base resistance R_{B1} 241 of the NPN transistor T1 231. The well/substrate resistance R_{B1} 241 appears between the substrate-tie 125 (which includes the P+ region 314) and the intrinsic base node of transistor T1 231. Likewise, the N-well 304 has an intrinsic resistance, which is observed as the base resistance R_{B2} 242 of the PNP transistor T2 232. The N-well or base resistance R_{B2} 242 appears between the intrinsic base node of transistor T2 232 and an optional N-well tie (not shown in Figure 3) that would be formed by a N+ doped region in the N-well 304. This N-well tie is optional, but it is left out (shown floating in FIG. 3) because it does not contribute to the function of the device. As such, the N-well tie is only needed for the PMOS triggered SCR having an N-well trigger tap G2 (see schematic diagram E of FIG. 2B). For either N-well or P-type substrates, the associated resistance is an inherent resistance. The well or substrate resistance value depends on the doping levels, as well as the length and cross sectional area of the N-well 304 and of the P-well 306/P-substrate 303. Typically, the well/substrate resistance R_{B1} 241 and R_{B2} 242 (if an N-well tie is

provided) have resistance values in a range of 500 to 5000 ohms for a silicon material.

[0046] Shallow trench isolation (STI) is used to separate regions that will receive high doping (e.g., regions 308, 312, and 314) as illustrated in FIG. 6. In particular, trenches are etched in specific areas, and an insulator material (e.g., silicon dioxide (SiO_2)) is illustratively deposited. The regions 308 and 312 may also be separated by other techniques known in the art, which are beneficial to the SCR operation.

[0047] N+ and P+ implant and annealing steps are conducted after the STI region formations to form the high-doped N+ and P+ regions, respectively. The implantations are done through separate photo masks for the N+ and P+ to allow the dopands to penetrate only into the dedicated regions of the IC 200.

[0048] Furthermore, a silicide layer 318 is formed over the N+ region 312 and P+ regions 308 and 314. In particular, a conductive layer (e.g., using cobalt, titanium, and the like) is formed on the surface of the IC 200. A silicide blocking-mask is provided to block unwanted silicide layers over certain areas of the IC. The silicide layers 318 serve as a conductive material respectively between each metal contact 121_A, 121_C, and 121_S (collectively metal contacts 121) at the anode 122, cathode 124, and substrate-tie 125. By using the silicide layers 318 only in certain parts of region 308 (for the anode 122) and region 312 (for the cathode 124), the risks of a shorting between the anode 122 and the surface of region 320_N, and between the cathode 124 and the surface of region 320_P (e.g., from thermal and mechanical stresses) is greatly reduced.

[0049] Specifically, looking from left to right in FIG. 3, a first STI region 316_1 is formed to the left of the first P+ doped region 308. Furthermore, a second STI region 316_3 is formed between the first N+ region 312 and the second P+ region 314, and a third STI region 316_4 is formed to the right of the second P+ region 314. As such, a surface region 309, which is located between the anode 122 and cathode 124, does not have any trench etched, high-doped regions, or insulative material deposited therebetween. Thus, the embodiment of FIG. 3 is different from the prior art (see STI region 116_2, N+ region 110, and the oxide layer 130 of

FIG. 1A). Accordingly, the entire device cross-section including the surface region 309, which extends over an N-well region 320_N and a P-well region 320_P (collectively non-high-doped region 320), may be utilized for SCR conduction.

[0050] Each of the high-doped regions (i.e., N+ region 312, and P+ regions 308 and 314) has a depth having a value "X_j", which is defined by the underlying semiconductor technology. In one embodiment, the depth X_j is in the range of 0.1 to 0.3 microns. Additionally, the distance from the silicided anode to the anode edge 311 has a length "A_j". Likewise, the distance from the silicided cathode 124 to the cathode edge 313 has a length "C_j". The lengths A_j and C_j are maintained within a particular range to reduce the possible detrimental impact of mechanical stress during the formation of the silicide 318, which could later lead to increased leakage currents. In particular, the physical lengths A_j and C_j are proportionally based on the height X_j of the P+ and N+ doped regions 308 and 312. The lengths A_j and C_j are in the range of two to five times the depth of the doped regions, where A_j and C_j are approximately equal. That is, A_j and C_j have values approximately in the range of $2X_j$ to $5\ X_j$. Preferably, the distance from the silicided anode to the anode edge A_j and distance from the silicided cathode to the cathode edge C_j is equal to approximately three times the height X_j of the doped regions 308 and 312. By maintaining such distances between the anode 122 and junction 307, as well as the cathode 124 and junction 307, the probability of stress related leakage currents and shorting of the silicide layers 318 is greatly reduced.

[0051] One objective of the present invention is to increase the speed in which the SCR 202 turns on. Recall that in the prior art, the N+ doped region 110 reduced the gain of the PNP transistor of the SCR because of the high recombination of the hole-electron pairs. Decreasing the turn on time of the SCR 202 is realized by two particular differences over the prior art. The first difference is a reduction in the size of the respective base regions of the transistors T1 231 and T2 232 in the SCR 202. The dimensions W_P and W_N in FIG. 3 represent the respective base widths of the NPN transistor T1 231 and the PNP transistor T2 232. The base widths W_N and W_P are respectively measured

from the edge 311 of the P+ region 308 to the junction 307, and from the edge 313 of the N+ region 312 to the junction 307. Reducing the size (i.e., base width) of the base of each transistor T1 231 and T2 232 of the SCR 202 reduces the time it takes for the minority carriers to diffuse through these regions and reach the corresponding collector regions. The transistors T2 232 and T1 231 preferably have as small as possible (as permitted by the semi-conductor process specifications) base widths W_N and W_P.

[0052] The SCR turn on time (SCR_{Ton}) is proportionally related to the combined base widths of each SCR transistor T1 231 and T2 232. In particular, the turn on time T_{on1} for the NPN transistor T1 231 is proportionally related to the square of the base width W_P of the NPN transistor T1 231. Likewise, the turn on time T_{on2} for the PNP transistor T2 232 is proportional to the square of the base width W_N of the PNP transistor T2 232. As such, the turn on time of the $SCR_{Ton} = ((T_{on1})^2 + (T_{on2})^2)^{1/2}$. Accordingly, since the base widths have been reduced compared to the prior art, the turn on time SCR_{Ton} has also been reduced.

[0053] The second difference over the prior art is the eliminated second N+ region 110. This reduces the overall doping level of the transistor T2 232 base (N-well 304). As such, the N-well 304, in the embodiment of FIG. 3, is able to provide an increase in current gain to the PNP transistor T2 232 of the SCR 202, since less electron-hole pairs will recombine during diffusion in the base region. The illustrative embodiment of FIG. 3 should be compared with the prior art of FIG. 1B. Referring to FIG. 1B, the high-doped N+ region 110 forms a part of the base of the PNP transistor T2 232, and thereby decreases the overall gain of the PNP transistor T2 232. This N+ region 110 provides high recombination of the minority carriers (holes) with the majority carriers (electrons), thereby resulting in the low amplifying characteristics of the transistor T1 231. Yet another problematic aspect with the prior art of FIG. 1B is the fact that the N+ region 110, the P-region 120, and the N+ region 112 form a relatively good lateral parasitic bipolar transistor close to the surface (not shown), as compared to the NPN transistor T1 231, which is situated deeper in the substrate / P-well 106. This surface NPN transistor is very well coupled through the common highly doped N+

region 110 to the deteriorated (surface) part of the PNP transistor T2 232. The prior art SCR device of FIG. 1B tends to remain in a state where only this parasitic surface NPN transistor conducts in the snapback mode. Furthermore, the PNP transistor T2 232 acts only as a forward biased base-emitter diode, while the deeper NPN transistor in the substrate (with lower current gain) does not trigger. As such, the prior art SCR device does not fully operate in the desired SCR mode due to its geometrical deficiencies. The prior art typically has 10% lower current handling capability. Additionally, due to the larger geometry, the prior device does not trigger safely and fast enough to protect very sensitive circuit elements.

[0054] Referring to FIG. 3, the shortening of the widths W_N and W_P of the transistor bases, and the elimination of the N+ region 110 decreases the trigger speed. Furthermore, the shortened widths W_N and W_P increase the overall gain of the transistors T1 231 and T2 232 in the SCR 202 by decreasing the hole-electron recombination effect caused by the presence of the N^+ region 110. The increased transistor current gains β help ensure that enough current is provided to forward bias the bases of each transistor T1 231 and T2 232, and thereby quickly and reliably activate the SCR 202.

[0055] The cross-sectional view in FIG. 3 illustratively depicts only the SCR 202 portion of the SCR ESD protection device 201, and does not depict the triggering device 205 of the present invention shown in FIG. 2. However, FIG. 4 illustratively depicts the triggering device 205 in conjunction with the SCR 202 of FIG. 3. Specifically, FIG. 4 depicts a top view of the NMOS-Triggered SCR ESD protection device 201 of FIG. 2A, and should be viewed along with FIG. 3.

[0056] In particular, FIG. 4 represents a top view of a portion of an integrated circuit 200 in which the triggering device 205 is external to the SCR 202, as compared to the prior triggering device 105 (see FIGS. 1A and 1B) being internal to the SCR 102. Furthermore, although the triggering device 205 and SCR 202 appear to be separate and distinct devices, they both are incorporated onto the same IC 200, and may be one of a plurality of ESD protection devices 201. In fact, a typical IC has numerous pads 148 that are each coupled to the internal

circuitry of the IC. As such, each of the pads 148 in the IC preferably has an ESD protection device 201, such as a NMOS triggered SCR, coupled thereon.

[0057] Referring to FIG. 4, the top view of the SCR 202 depicts the N-well region 304 and the P-well region 306. In particular, a single P+ region 308 in the N-well 304 forms the anode 122. A plurality of metal contacts 121_A connect the anode 122 to the pad 148. The pad 148 is also coupled to the protected circuitry of the IC 200, optionally through the current limiting resistor R_L. A portion of the P+ region 308 beneath the metal contacts 121_A is covered by the silicide 318_A as discussed above in reference to FIG. 3. Furthermore, the distance A_j as discussed above is also shown in FIG. 4.

[0058] The cathode 124 is formed from N+ regions 312_1 through 312_m (collectively N+ region 312). A plurality of metal contacts 121_C connects the cathode 124 to ground. A portion of each (interspersed) N+ region 312_m beneath the metal contacts 121_C is covered by a corresponding silicide layer (e.g., silicide layers 318_{C-1} and 318_{C-m}) as discussed above in reference to FIG. 3. Furthermore, the distance C_j is also shown in FIG. 4.

[0059] Disposed in the vicinity of the N+ regions 312 is a trigger tap 401. The trigger tap 401 is formed by a P+ region 402 having a silicide layer 418_T disposed over a portion of the P+ region 402, and one or more metal contacts 121_T disposed over the silicide layer 418_T. Furthermore, the illustrative trigger tap 401 may be one of a plurality of trigger taps, with a P-well spacing 404 defined therebetween.

[0060] Specifically, the P+ region 402 of the trigger tap 401 is disposed in close proximity to the N+ regions 312. Preferably, the trigger tap 401 is also aligned with the N+ regions 312. By disposing the trigger tap 401 in close proximity to the N+ regions 312, the base resistance from the trigger tap to the intrinsic base node of the NPN transistor T1 231 is reduced. The P-well spacing 404 is defined by the P-well material 306 and is preferably minimal in size. The P+ region 402 of the trigger tap 401, combined with the adjacent P-well spacing 404 and the N+ regions 312 together form a diode, which is forward biased when a positive voltage appears on the P+ region 402. In particular, the triggering

device 105 acts as a current source at the base of the NPN transistor T1 231, by injecting majority carriers (holes) into the P-type base material, which forward biases the base-emitter (P-well spacing/region 404/306 and N+ 312) of the NPN transistor T1 231. Furthermore, for normal circuit operation (i.e. no ESD event), the close proximity of the trigger tap 401 to the SCR 202 and the N+ emitter regions 312 of the SCR 202 is advantageous as will be described in hereafter. Unintended triggering of an SCR by certain circuit over-voltage conditions is known to disrupt the circuit (e.g., cause a Latch-Up condition). As the trigger tap is grounded through the shunt resistor 210, the p-well 306 of the SCR receives additional coupling to ground, which will prevent Latch-Up.

[0061] The STI regions 316 circumscribe the SCR 202 and the trigger device 205 such that the anode 122, cathode 124, and portions of the SCR 202 therebetween are not covered with the STI material as discussed above with regard to FIG. 3. In particular, the doped P+ region 308, intermittent N+ regions 312, the surface area 309 between the P+ and N+ doped regions 308 and 312, the trigger taps 401, and the P-well spacing 404 do not have any STI 316 disposed thereupon in this preferred embodiment. However, the P-well spacing 404 may also be covered with STI as only negligible influence on the diodes (402-404-312) takes place. As such, the combination of the area-reduced layout from omitting the N+ region 110 and the gate 126, and the trigger taps 401 introduced in-line with the N+ regions 312 (emitter of the NPN transistor T1 231) results in faster triggering of the SCR 202 of the present invention.

[0062] In the embodiment shown in FIG. 4, the grounded local substrate ties 125 are preferably located at maximum distance from the N+ regions 312, and are separated by the STI region 316_3. Alternately, the SCR 202 may have a closed ring P-substrate tie (not shown) circumscribing the SCR 202 that is grounded. The distance of P-substrate ring from the SCR 202 and the trigger device 205 may be at a range from 2 to 20um, preferably larger than 5um. As such, the trigger taps 401 are positioned away from either the closed ring P-substrate tie and the local substrate ties 125 to avoid current leakage to ground. Specifically, the trigger taps 401 are in line and in close proximity to the N+

regions 312, since alternately locating the trigger taps 401 near a grounded P-substrate tie would disadvantageously result in current leakage from the P+ region 402 to ground. Such current leakage to ground subtracts away from the current required to forward bias the transistors in the SCR 202, which may delay or thwart activation of the SCR 202.

[0063] In one embodiment, the triggering device 205 is illustratively the NMOS transistor 206. Referring to the schematic diagram A of FIG. 2A along with FIG. 4, the NMOS transistor 206 is an on-chip transistor external to the SCR 202. The drain of the NMOS transistor 206 is coupled to the pad 148. The source of the NMOS transistor 206 is coupled to one end of the resistor 210, as well as to the trigger tap 401 adjacent to N+ regions 312 of the cathode 124. Additionally, the other end of the resistor 210 is also tied to ground. Moreover, the gate 126 of the NMOS device 205 is connected to the source of the NMOS 205 and is effectively coupled to ground through the resistor 210.

[0064] The resistor 210 has a selected resistance value in the range of 100 Ohms to 2000 Ohms, which is substantially lower than the inherent resistance of the P-substrate 302 and P-well 306. The latter may be in a range of several kilo Ohms depending on the location of the P+ substrate ties 125. As such, those skilled in the art will appreciate that resistor 210 can easily control the total resistance to ground, and thus control triggering and holding current of the SCR. Furthermore, any leakage currents from the trigger device 205 are shunted to ground via the path through this resistor. In one embodiment, the resistor 210 is fabricated from a silicide-blocked poly-silicon, because the poly-silicon sheet resistance value allows easy dimensioning of the desired resistor value and because the poly-silicon resistor 210 is completely isolated from the substrate 30by the STI. Moreover, those skilled in the art will understand that any other resistive material that is available in the IC manufacturing process may used as well.

[0065] In the illustrative embodiment shown in FIG. 4, the trigger device 205 (e.g., NMOS trigger) is fabricated from the N+ material, and also features silicide blocking to ensure that the trigger device itself will be ESD robust, while still

providing the trigger current to the SCR 202. In particular, silicide layers 418_S and 418_D are respectively disposed over the source and drain of the NMOS trigger device in areas where the contacts 421_S and 421_D are positioned.

[0066] In operation, the trigger current is provided by the external NMOS trigger device 205, and is injected into the trigger taps 401 of the SCR 202. Specifically, the external triggering current is provided from the source of the NMOS trigger device 205, which goes into breakdown, and subsequently into snapback. The NMOS trigger device 205 ensures a low trigger voltage of the ESD protection element, since the trigger voltage is determined by the drain-substrate breakdown voltage (e.g., 8 volts) of the NMOS transistor 206, and not by the intrinsically high breakdown voltage of the SCR 202 (in the range of 15 to 25V). The trigger current is injected as a base current into the base of the NPN transistor T1 231. As such, the inventive embodiment, as shown in FIGS. 2-4, differs from the prior art LVTSCR of FIGS. 1A and 1B, where the trigger current is injected by an internal source into the base of a slow acting PNP transistor T2 232.

[0067] As discussed above, the inventive trigger device 205 and SCR 202 are respectively depicted as a NMOS triggering device. However, one skilled in the art will recognize that a PMOS triggered SCR structure for ESD protection may be utilized. For purposes of completeness of illustrating the present invention, FIG 2B depicts an illustrative schematic diagram of a grounded gate PMOS (PMOS) triggered SCR ESD protection device of the present invention, and FIG. 5 depicts a top view of the PMOS-triggered SCR ESD protection device of FIG. 2B. Referring to FIG. 5, the layout of the triggering device 205 and SCR 202 are the same as illustrated in FIG. 4. However, the N-type and P-type materials are reversed. That is, wherever a N+ or N-type material is shown in FIG. 4, a P+ or P-type material is respectively depicted in FIG. 5. Likewise, wherever a P+ or P-type material is shown in FIG. 4, a N+ or N-type material is respectively depicted in FIG. 5. However, the P-substrate 302, as shown in FIG. 3, remains the same for both embodiments of FIGS. 4 and 5. As such, additional P+ substrate ties (e.g., substrate-ties 314_{C1} and 314_{CS}) are placed near the N+

region 318_C or a closed P+ substrate ring (not shown) is placed around the entire structure. The PMOS triggering device 205 is fabricated from P+ type material and placed in an N-well, and the trigger tap 401 is fabricated from a N+ type material, in contrast to the reversed embodiment shown in FIG. 4.

[0068] In normal operation of the IC, the PMOS gate is tied high together with the PMOS source through the external resistor 210 such that no MOS-current will flow through the source to drain channel. When a positive ESD event with an excessive voltage occurs at the pad, an avalanche breakdown occurs between the drain and the N-well junction above a predetermined threshold voltage (e.g., 8 to 10 volts), and the PMOS transistor will operate as a parasitic, lateral PNP transistor. Consequently, current will flow through the PMOS device and the voltage across the source and drain terminals will drop to a lower value. The gate G2 (schematic drawing E in FIG. 2B) is then pulled low, and the SCR 202 turns on. The gate G2 is identical with the trigger taps 401 in FIG. 5. A voltage drop forms across the intrinsic N-well resistance R_{B2} 242 and across the external resistance 210. Since the external resistance 210 has a resistance value of 100 Ohms to 2000 Ohms, that is much less than the intrinsic N-well resistance R_{B2} value (500 Ohm to 5000 Ohms), the external resistance 210 functions as a current shunt to control and tune the trigger and holding currents of the SCR 202. As such, the triggering of the ESD protection device 201 shunts the discharge current during a positive ESD event at the pad to ground, and therefore limits the transient voltage drop to a value that is tolerable by the circuitry of the IC 200.

[0069] FIG. 6 depicts a cross-sectional view of a second embodiment of a SCR 602 of the NMOS-triggered SCR ESD protection device 201. Specifically, FIG. 6 represents an SCR 202 that is fully silicided over the P+ and N+ regions 308 and 312. The base widths W_N and W_P of the transistors T2 232 and T1 231 are shown, respectively. Furthermore, shallow trench isolation (STI) is disposed over the entire SCR 202 as shown by STI regions 316_1, 616, 316_3, and 316_4. In particular, the STI region 616 is disposed on the surface area 309 between the silicided layers 618_A and 618_C. Accordingly, the STI region 616 serves as an

isolator between the anode 122 and cathode 124 to prevent shorting between the respective silicide layers 618_A and 618_C.

[0070] Moreover, the respective base widths W_N and W_P of the transistors T2 232 and T1 231 are determined by the length of the STI region 616. In particular, during manufacturing of the IC 200, the STI material is selectively deposited over the SCR 202. Thereafter, the P+ and N+ doped regions 308, 312, and 314 and respective silicide layers 618_A, 618_C, and 618_S are formed. As discussed with regard to the embodiment of FIG. 3, reducing the lengths (i.e., widths) of the base regions means that the overall distance in which the minority carriers must diffuse through these base regions is reduced. In the second embodiment shown in FIG. 6, the base widths W_N and W_P for the respective transistors T2 232 and T1 231 are typically slightly smaller than in the embodiment depicted in FIG. 3. As such, this second embodiment depicted in FIG. 6 differs from the prior art of FIG. 1B, since the high-doped N+ region 110 from the triggering device 205 is eliminated and very compact dimensions of the SCR can be realized for fast turn on. Moreover, the embodiment depicted in FIG. 6 is an alternative and a further improvement over the embodiment depicted in FIG. 3, because it consumes less silicon area. That is, all high-doped regions 308, 312, 314, and the trigger tap 402 (see FIG. 4) are fully silicided.

[0071] Furthermore, by utilizing a triggering device 205, which is also fully silicided and covered with the STI, wafer processing costs may be reduced because the additional and costly procedure of silicide blocking is not required. In particular, a back-end-ballasted, NMOS (BEBNMOS) device may be used as triggering device. Such BEBNMOS device is disclosed in US application S/N 09/583/141, entitled "Apparatus For Current Ballasting ESD Sensitive Devices", Attorney Docket SAR13663, filed May 30, 2000, and is incorporated by reference herein in its entirety.

[0072] FIG. 7 depicts a cross-sectional view of an external back-end ballasted, NMOS (BEBNMOS) trigger device 705. A plurality of ballasting resistors 730 and 731 (only one of each shown in FIG. 7), extends from the drain 714 and source 716 of the trigger device 705, and is used to separate electrically

isolated ballasted current paths between the external contact and the contact electrodes of the ESD device, or the current carrying device being protected. These isolated ballasted current paths advantageously include in part, distributing current more evenly than other prior art devices, reducing current crowding, which in turn, reduces the localized heating of the ESD device, ballast resistance linearity, lower permissible values of ballast resistance, no added junction capacitance, more compact layout, no extra process steps as with silicide blocked devices, and the like.

[0073] Referring to FIG. 7, the source 716, drain 714, and gate 718 regions of the BEBNMOS trigger device 705 are formed by conventional fabrication processes known in the art. Specifically, the BEBNMOS trigger device 705 comprises a P-well 710 having a STI region disposed over the surface of the P-well 710. The gate 718 is disposed over a P-channel 723 and may illustratively be formed by a polysilicon layer disposed over a silicon dioxide layer, as discussed above with regard to FIG. 1B. The silicon and polysilicon are highly N doped semiconductor regions to form the N+ source region 720_S under the source electrode 716 and the N+ source region 720_D under the drain electrode 714, such that a P-channel 723 is formed between the source 716 and drain 714.

[0074] A single vertically meandering strip 730 illustratively connects to a common terminal 732_D to the drain region of the device 705. Following the path of the strip 730 and starting at the external common terminal 732_D, the strip 730 includes a metal contact 734_1, down to a segment of polysilicon 736, up to a second metal contact 734_2, to a first metal layer 738, to a first via 740, to a segment of a second metal layer 742, to a second via 744, and to a segment of a third metal layer 746. The segment of the third metal layer 746 is connected to a second segment of the polysilicon layer 736 through a series connection of a via, a segment of the second metal layer 742, another via, a segment of the first metal layer 738, and another metal contact. This second segment of polysilicon is connected to a second segment of the third metal layer 746 through a metal contact, a segment of the first metal layer 738, a via, a segment of the second metal layer 742, and another via. Finally, in this exemplary embodiment, the

second segment of the third metal layer 746 is connected to the drain region 714 of the ESD device 705 through a series connection of a via, a segment of the second metal layer 742, another via, a segment of a the first metal layer 738, and a connecting metal contact 748.

[0075] In the exemplary embodiment of the BEBNMOS triggering device 705, the first, second, and third metal layers 738, 742, and 746 may be fabricated from aluminum or copper films and the vias and connecting metal contact may be tungsten plugs or copper. These series connections form the ballasting resistor 730. In this embodiment, each of the vias and the metal contact adds a significant resistance (e.g., 5 to 10 ohms in advanced deep sub-micron technologies) and each of the segments of the polysilicon layers 736 add a significant resistance (e.g., 40 to 80 ohms in advanced deep sub-micron technologies) to the ballasting resistor 730. Each of the other layers also adds resistance to the ballasting resistor 730. However, the resistance of the metal layers 738, 742, and 746 is negligible as compared to the combined resistance of the polysilicon layers 736, the connecting metal contacts 734, and the vias 740.

[0076] Furthermore, a similar ballasting resistor 731 is formed over the source 716 of the BEBNMOS triggering device 705. However, the resistance is typically less than the resistance at the drain 714. In particular, less metal layer segments 738, 742, and 746, vias 740, polysilicon layer segments 736 and metal contacts 734 are utilized. Moreover, one skilled in the art will recognize that a satisfactory ballasting resistor may be fabricated using more or fewer layers and/or more or fewer meanders.

[0077] FIG. 8 depicts a top view of a ballasted, NMOS (BEBNMOS) triggered SCR ESD protection device 800. The BEBNMOS triggered SCR ESD protection device 800 comprises the SCR 202 of FIG. 3 or the SCR 602 of FIG. 6 coupled to the BEBNMOS trigger 705 of FIG. 7 and the external shunt resistor 210. In particular, the BEBNMOS trigger 705 has a plurality of the ballasting resistors 730_j coupled from the drain 714 to the external connector 732_D. The external connector 732_D is then coupled to the pad 148. Similarly, the BEBNMOS trigger 705 has a plurality of the ballasting resistors 731_K coupled from the source 716 to

the external connector 732_S. The external connector 732_S is then coupled to one end of the shunt resistor 210. Each ballasting resistor 730 and 731 is illustratively fabricated with the meandering, non-intersecting strips in the manner described above in FIG. 7, and are separated from each other by spacings 740_1 through 740_{K-1} on the drain region 714, and by spacings 741_1 through 741_{K-1} on the source region 716.

[0078] The remaining circuitry of the BEBNMOS triggered SCR ESD protection device 800 is the same as described with regard to the embodiment in Fig. 6. As such, BEBNMOS trigger 705 and SCR 602 of the ESD protection device 800 have the STI 316 disposed over the entire surface area of the SCR, except for the high-doped anode 122, cathode 124, substrate ties 125, and trigger tap 401 regions 308, 312, 314, and 402, respectively, that are fully silicided.

[0079] The embodiments depicted in FIGS. 2-8 illustratively show that by using the carefully chosen trigger taps in conjunction with an external triggering device 205 (e.g., NMOS trigger), the base widths of the transistors T1 231 and T2 232 in the SCR 202 can be reduced. As such, the triggering speed of the SCR 202 is faster and triggering more reliable, as compared to the prior art ESD protection devices, while the current gain is increased. Fast triggering is a key to prevent trigger voltage overshoots as they occur in slow SCRs. Therefore, the fast SCRs of the present invention can successfully limit the transient voltage during an ESD to such a level that the ultra-thin gate oxides (less than 7nm) of deep sub-micron processes are protected while prior art devices clearly show deficiencies.

[0080] Although various embodiments that incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.